

CM6531N_CM9600 USB Audio

USB Audio

Low Power for Headset / Microphone / Docking

Application Notes

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Release Note

Revision	Date	Description
1.00	2014/5/27	First release
1.1	2014/9/17	Modify Ch2.2 description.
1.2	2014/11/20	Add Notice! For default have no function.
1.3	2014/12/30	Fix 3.6~3.7 table issue & modify Cap-less description & some issue
1.4	2015/05/18	Correct typing error.
1.5	2024/08/15	Add CM9600 CODEC.

1 About This Document

The purpose of this document is to summarize the common application notes for customers who are designing their products with Cmedia CM6531N USB audio processor series or who are evaluating the solutions. It will contain the following contents about the typical system block diagram; schematics design notes, layout guide, applicable PC OS & Apple IOS & Android, and exception notes. It's recommended to read this document before you start to plan and design your products with CM6531N USB audio solution.

2 Schematics Design Notes

2.1 Test Pin for firmware crash recover

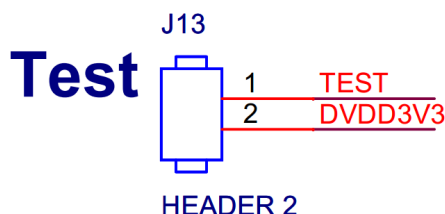


Figure1. CM6531N Test Pin circuit.

When CM6531N firmware crashed, short Test Pin to 3.3V re-plug in PC could into Test Mode (Flash recover mode).

Notice!! CM6531N series default firmware is empty and have no function!! The device PID/VID always = 0D8C/0018.

When plug into pc will show

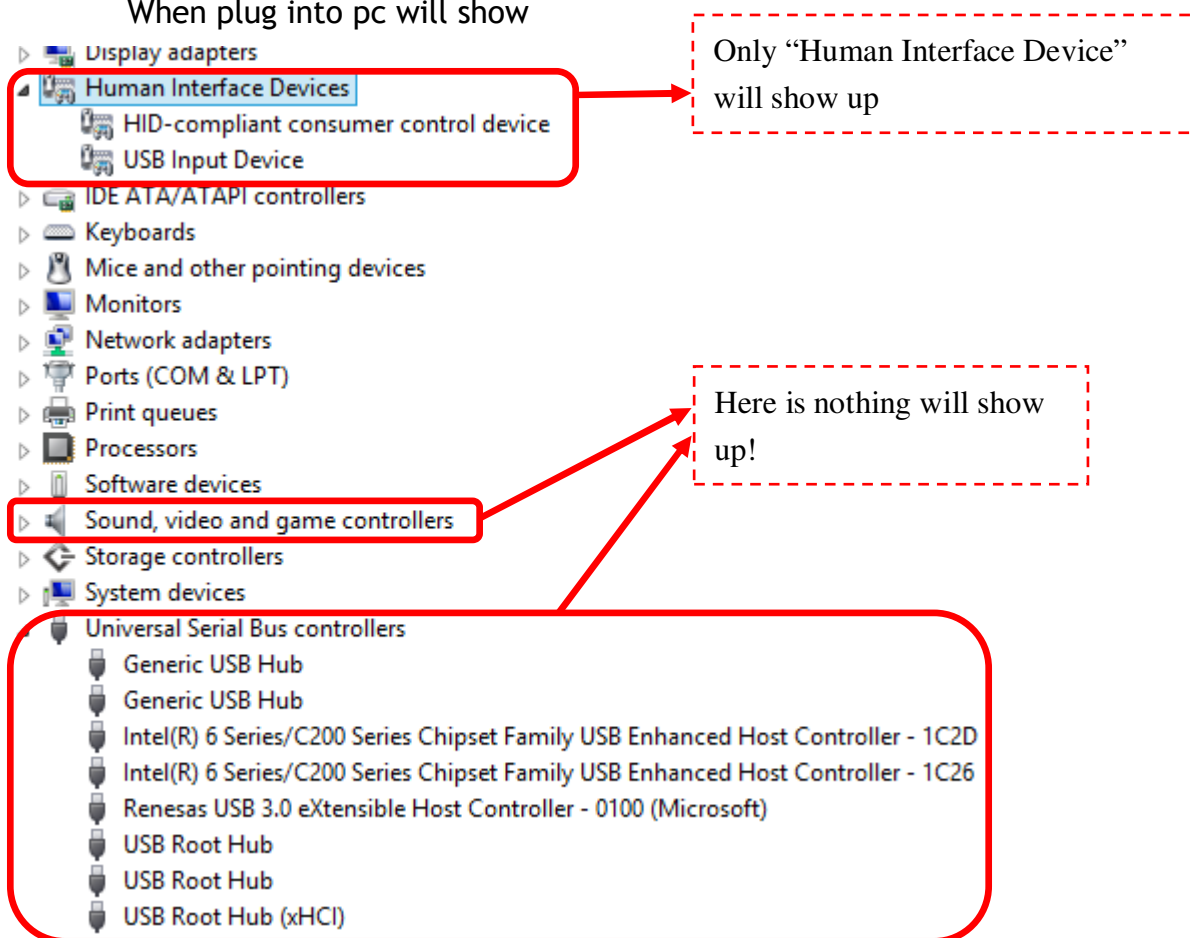


Figure1. CM6531N default only have HID function.

2.2 Power Control Design

Power Control

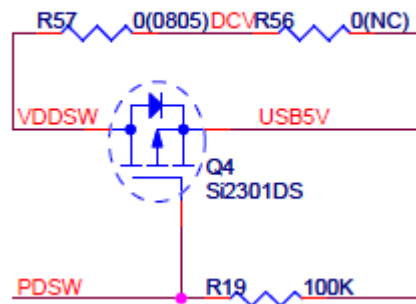


Figure2. CM6531N power control circuit.

PDSW pin support DC 1.8V ~ 5V

OS Mode	PDSW	VDDSW
Operation	Drive Low	5V
Suspend	Open	0V

2.3 Crystal Design

Crystal

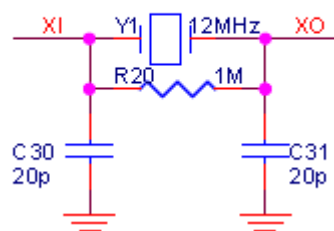


Figure3. CM6531N crystal circuit.

For i-Device low power mode & I2S need a 12MHz/30ppm Crystal.

2.4 USB Interface Design & GND Separate Design

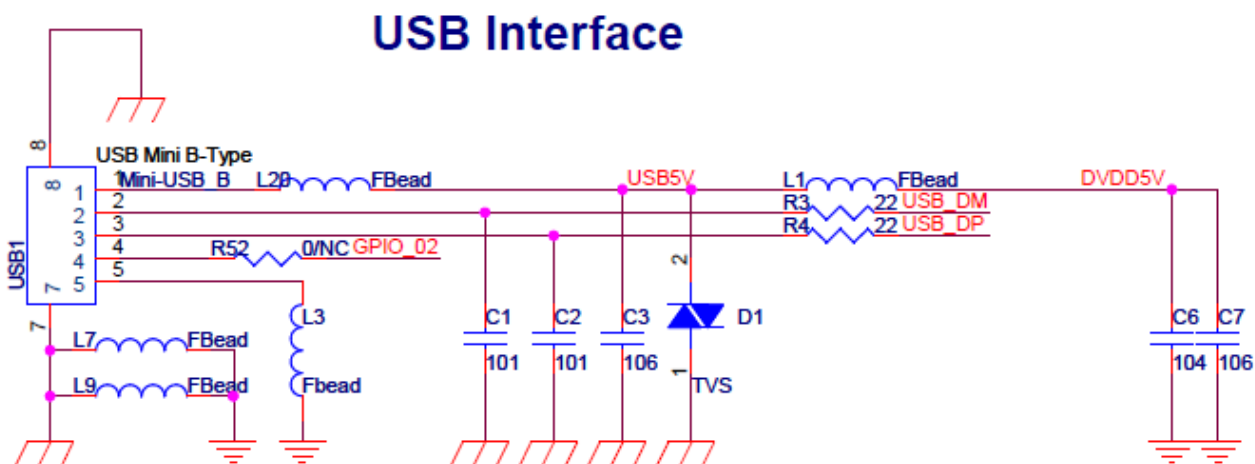


Figure4. CM6531N USB & GND separate circuit.

R3 & R4 for USB phy impedance matching.

C1 & C2 for EMI solution.

D1, for ESD solution.

Digital GND  & Shielding GND  separate by 0ohm (0805).

USB TVS(D8, D9) Choose Suggest

Device Descriptio	Rising Time	Data Rate	Suggested capacitor
USB 1.1	4-20 nS	12 M bps	3-40pF

2.5 EQ Select Design (default disable; need firmware enable)

EQ Select

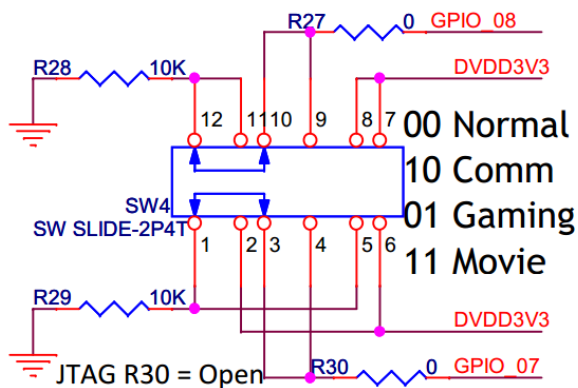


Figure5. CM6531N EQ switch circuit.

SW7 is a multi switch to set EQ0, EQ1 value.

GPIO 8	GPIO 7	Mode
0	0	Normal mode
0	1	Gaming mode
1	0	Communication mode
1	1	Movies mode

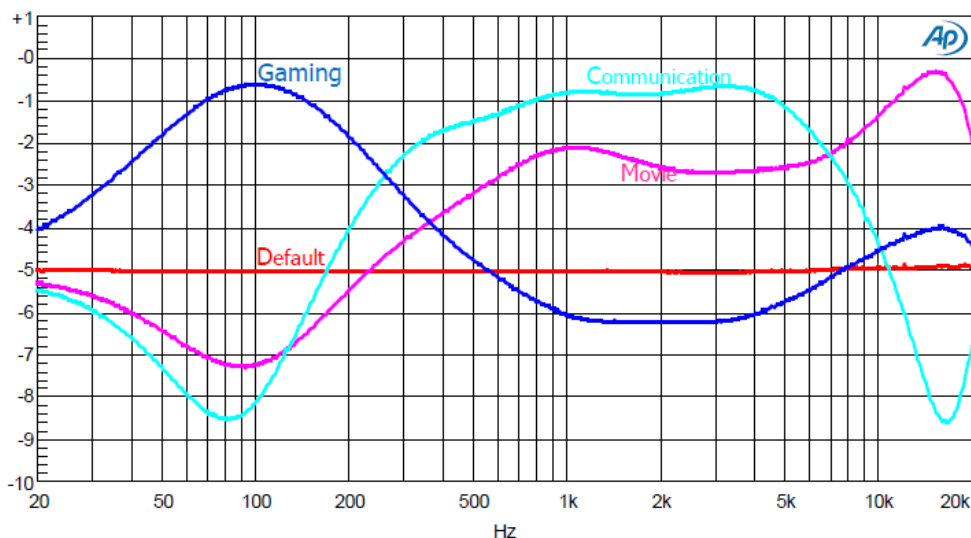


Figure6. CM6531N default support EQ mode frequency response.

The EQ select function control by firmware, and default is disable.(CM6531N demo board not support)

2.6 HID Button

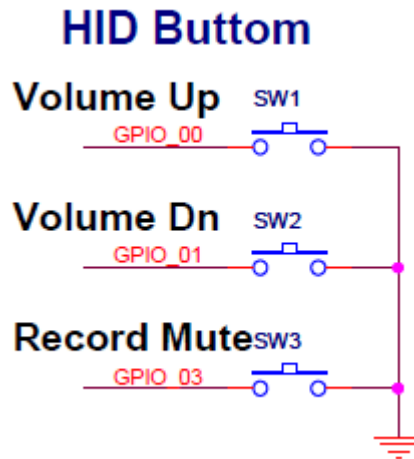


Figure7. CM6531N HID Button circuit.

CM6531N Support HID Button. Use CM6531N GPIO (default pull high), when push the button will drive low, and trigger firmware report function to OS.

Default support:

- Volume Up, (DB support)
- Volume Down, (DB support)
- Play Mute (Need Firmware Support)
- Record Mute.(Self Mute) (DB support)
- Play/Pause(Need Firmware Support)
- Next(Need Firmware Support)
- Previous(Need Firmware Support)
- Stop(Need Firmware Support)

2.7 3 Color LED

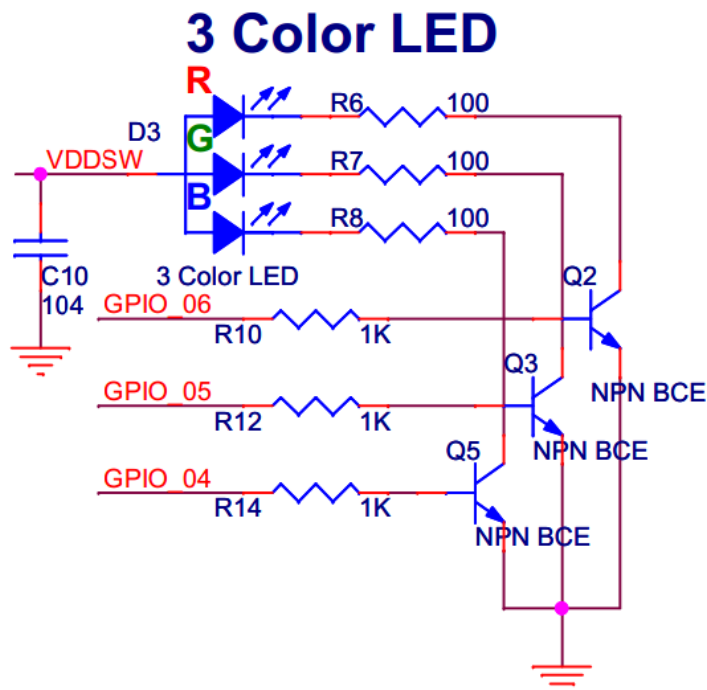


Figure8. CM6531N Common-anode high brightness 3 Color LED circuit.

Common-anode 3 Color high brightness LED(20mA each LED) control need a NPN transistor(Q2, Q3, Q5) provide higher power. And GPIO 04~06 is PWM signal, layout must follow layout guide.

CM6531N Support 3 color(Red, Green, Blue) LED , need firmware program it. (i-Device not support, cause current limit only 100mA)

2.8 DC to DC Power Design

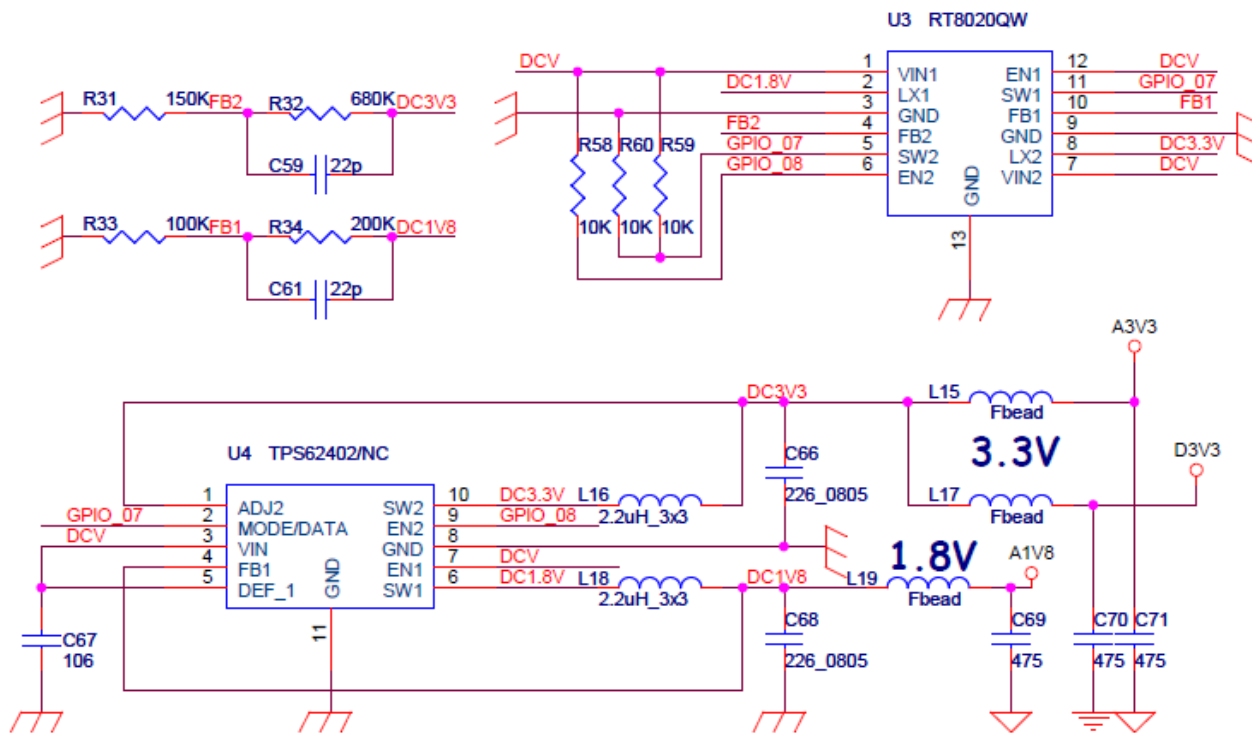


Figure9. CM6531N DC to DC power control circuit.

For i-Device low power mode need a DC to DC provide 3.3V(for higher power efficiency).(The demo board is U3)

The DC to DC power had much switching noise, so the layout must be note. GND Must

connect to shielding GND 

2.9 3.3V(Apple device) & 5V(PC/Android) Detect

3.3V & 5V Detect

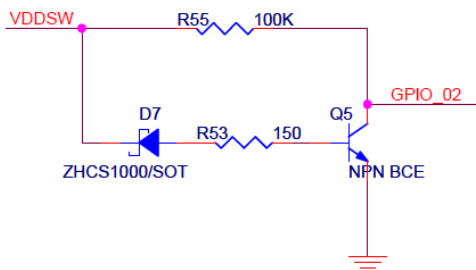


Figure10. CM6531N i-Device(3V3) or PC(5V) Detect circuit.

When CM6531N plug in i-Device(iPod touch5, iPhone5/ 5S/ 6/ 6+/, iPad / 4/ 5/ mini/Air...) it provide 3.3V power. The VDDSW = 3.3V & the zener diode(4.7V) won't be turn on so PNP transistor "C" = VDDSW(Q5 = off) When CM6531N plug in PC/ Android , it provide 5V power. The VDDSW - 5V & the zener diode(4.7V) will be turn on so PNP transistor "C" = low (Q5 = on).

Firmware will detect the GPIO_02, when GPIO_02 = High, iAp will detect by Apple device; GPIO_02 = Low, PC / Android won't detect.

2.10 i-Device License IC (CP)

iDevice IC (CP)

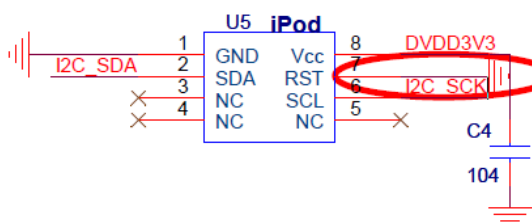


Figure11. CM6531N i-Device license IC circuit.

For Apple device (i-Pod touch5, i-Pad 4~i-Pad Air, i-Phone 5/5S/6/6+...other support lightning connector & IOS 7 or letter Apple device).

2.11 Crystal Circuit

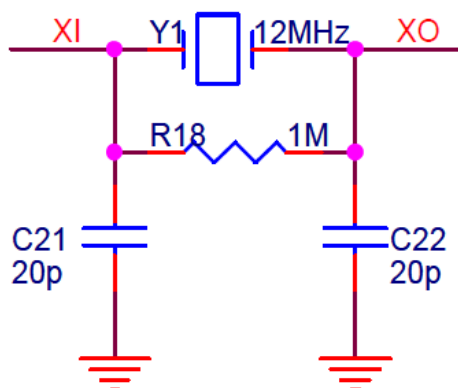
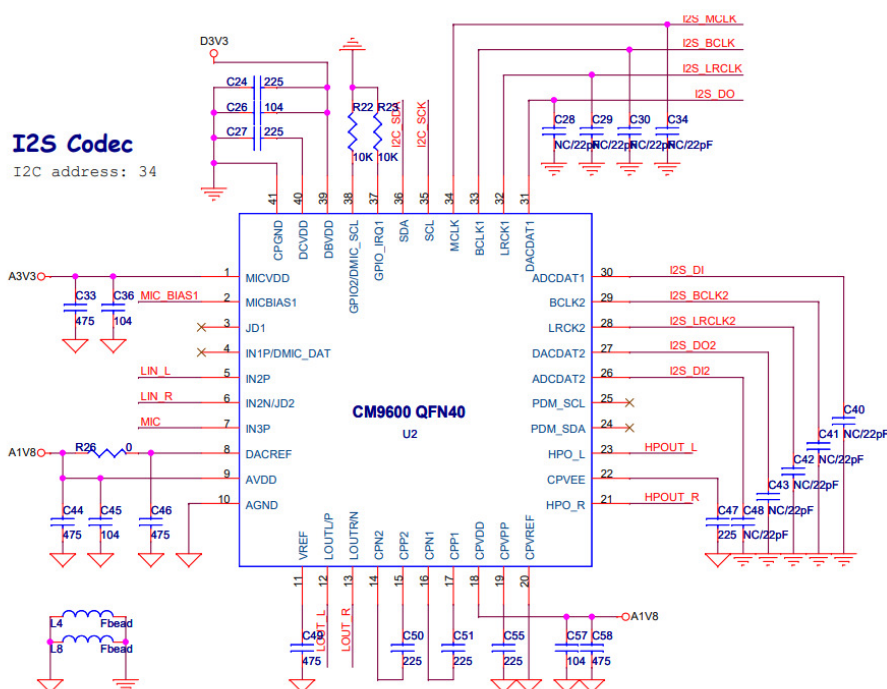


Figure12. CM6531N Crystal circuit.

The crystal circuit can save USB bus power.

2.12 CODEC CM9600

The CM9600 is a high performance, low power, dual I2S interface audio CODEC. First I2S interface can support dual mode: normal I2S and I2S with TDM (Time Division Multiplexing) interface. The TDM interface can transmit/receive up to 8 channels data. The transmitted data can from analog input or digital microphone input. Also the received data can to headphone output, line output or PDM output.



3 Layout Guide

This document provides guideline for the design of USB audio PCB. It’s important to ensure maximum performance proper component placement and routing. This document includes properly isolated digital circuitry and analog circuitry. The effects of ground loop and supply plane geometry, decoupling/ bypassing/ filtering capacitors placement priorities, USB D+ and D- signals, analog power supplies, and analog ground planes.

3.1 General Rules

1. If it's necessary to turn 90°, it's better to use two 135° turn (keep angles $\geq 135^\circ$) or an arc, instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.

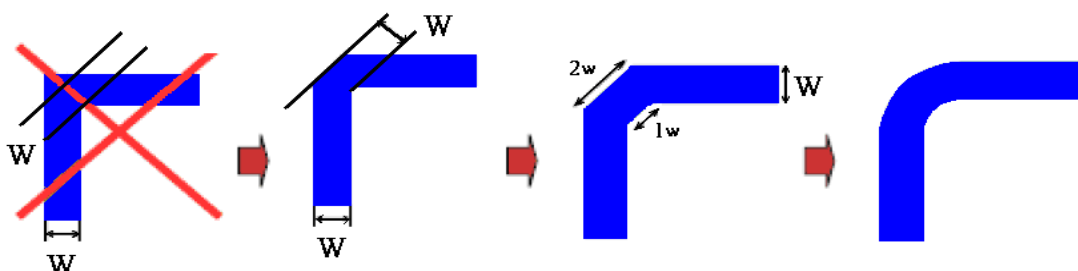


Figure11. Turn angle.

Figure11. Turn Angle

2. The old rules of splitting power and ground into “digital” and “analog” sections do necessarily apply to the many audio devices. AGND and APWR plane as the same region as possible, place DGND and DPWR plane on other region.
3. Use Ferrite Bead to connect different ground plane to avoid the EMI issue.

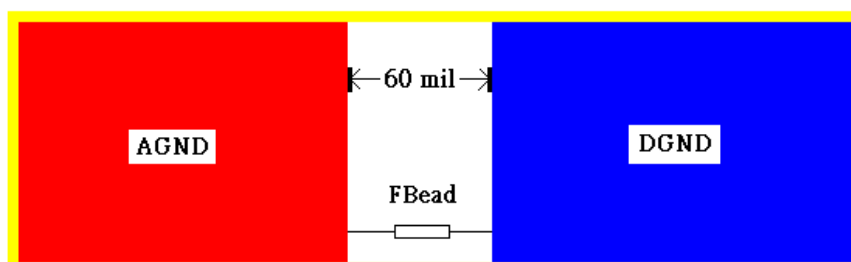


Figure12. AGND & DGND.

4. Connect analog and digital power planes at one point through a low impedance bridge or preferably through a ferrite bead.
5. To achieve proper ESD/EMI performance; it's suggested to use a 0.1uF capacitor on each cable PWR bus line to chassis GND close to the connector pin. If voltage regulators are used, place a 0.1µF capacitor on both input and output. This is to increase the immunity to ESD and reduce EMI.

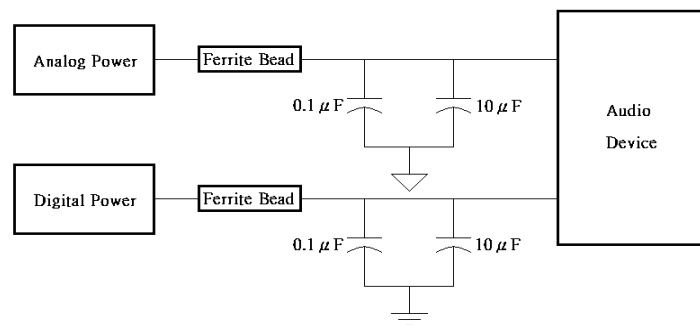


Figure13. Capacitors array.

6. Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

3.2 Differential Signal Pair Impedance Matching

The USB D+ D- differential pairs, which can operate at a rate of 12Mbit/s, are some of the most critical signals on a PCB. Its implementation on the PCB requires special considerations. The inductive and capacitive reactance, resistance, and conductance of a PCB differential pair will determine the impedance of the trace pair at any point along the PCB track. The value of differential impedance will be a function of the physical dimensions of the trace, as detail below.

Differential: Impedance of 90Ω, is optimal

Single-end: Impedance of 45Ω, is optimal

1. Place CM6531N USB Audio Controller chip as close as to the USB connector and place it on the un-routed board first, with minimum trace lengths, as equal as possible, route full-speed differential signal pair first. Keep appropriate distance between full-speed signals to USB differential signal pair.
2. Route the USB differential signal pair on the component side, which is adjacent to the ground plane layer. Vias to different signal trace layers or routing too close to breaks in the ground plane will adversely affect the differential trace impedance.
3. Route USB differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change.
4. Please don't route USB differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference.

- Stubs on USB differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality.

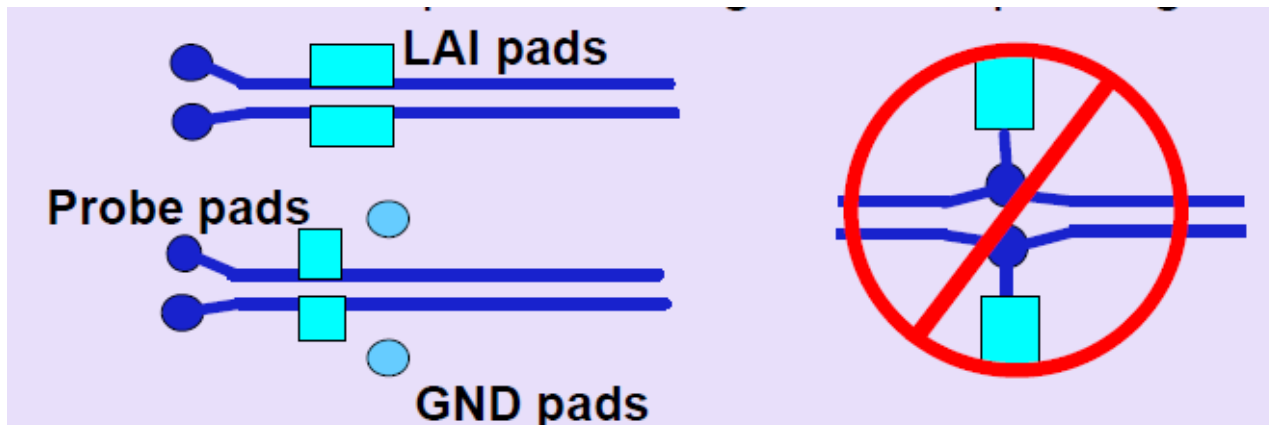


Figure14. Stubs affect.

- Route USB differential signal pair traces over continuous ground and power planes. Avoid differential signal pair crossing anti-etch areas or any break in the underlying planes and routing the near the edge of the PCB or power planes.

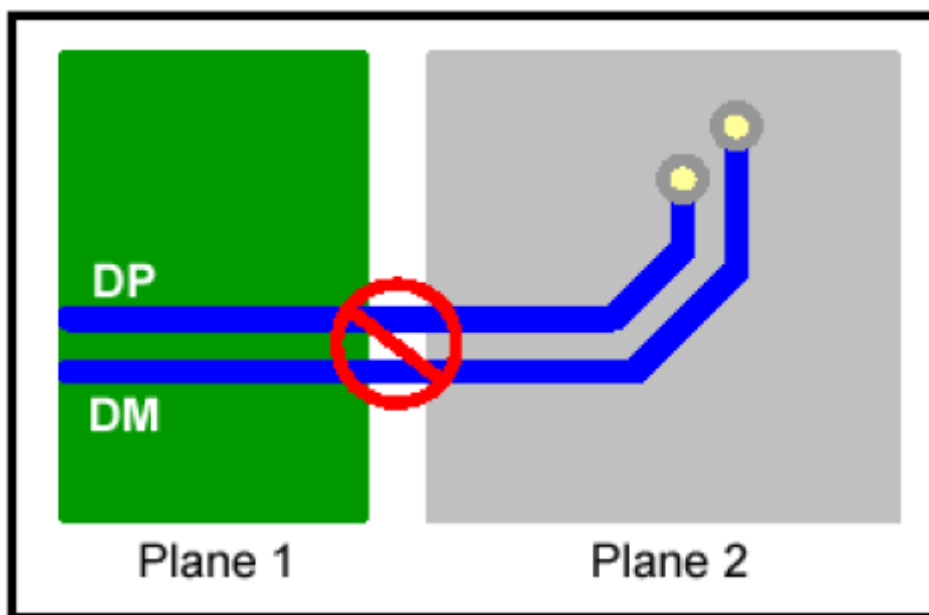


Figure15. Route USB traces fail.

- Keep parallelism between PERp0/PERn0; PETp0/PETn0 and REFCLK+/REFCLK- with the same trace spacing, which achieves 100Ω differential impedance.
- Route paths of SPDIF IN and OUT to separate t least 20 mils gap.

9. Do not allow any digital or analog signal traces pass through the drawbridge, otherwise, the digital noise may induced into the analog signals, makes audio performance worse.
10. Avoid crossing the image power or ground plane boundaries with full-speed clock signal traces immediately above or below the separated planes. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through screw holes.
11. Cmedia recommended to layout the width of each signal traces at least 10 mils and the space is the least one time the size of width of signal trace.
12. For ADC and DAC, VREF is also bypassed. Depending upon the converter architecture, the range of the large capacitor may be from 1uF to 47uF. Place bypass capacitor near chip.
13. Placement of the capacitor near the chips is very important. The bypass capacitors provide full speed current for the modulator operation, so the bypass capacitors are actually used to store charge for this full speed current draw.

3.3 Layout design of Ground and Supply Plane geometry

The layout separates the analog and digital ground planes with a 60 to 100 mils gap. The moat helps to isolate noisy digital circuitry from clean analog audio circuitry. The digital and analog ground planes are tied together by a wide link (about 50mils) at a point close to the USB connector. This will be the "drawbridge" that goes across the moat. Do not allow any digital or analog signal traces pass through the drawbridge. Otherwise, the digital noise may get into the analog signals and make audio performance worse.

In order to achieve the best audio performance and prevent crosstalk issue, Cmedia recommend that the width of each I/O signal trace be at least 10 mils and the space be at least one time the size of the width of signal trace.

For a layout that helps to reduce noise, separating analog and digital ground planes is needed. The digital components should be placed over the digital ground plane, and the analog components (including the analog power regulators) should be placed over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their ground planes. Place analog power coincident with analog ground and digital power coincident with digital ground. If any portion of analog and digital plane overlaps, the distributed capacitance between the

overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolating the power planes. The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

3.4 Decoupling and bypassing capacitors

Bypass capacitors on the PCB are used to short digital noise to ground. Commonly, USB audio controller may generate noise when its internal digital circuitry is operating. The current changes arise in the power and ground pins for the related section of the USB audio controller. The goal is to force AC current to flow in the shortest loop from the supply pin through the bypass cap and back into the USB audio controller through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the USB audio controller and the bypass capacitors when in the operating frequency of the USB audio controller. The long-trace will greater the inductance. To avoid long-trace inductance effects, use the shortest traces for bypass capacitors, with wide traces to reduce impedance. For the best performance, use supply bypass leads of less than one-half inch.

The USB audio controller power supply pins are need the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10 μ F surface mount devices are good if they are used in conjunction with 0.1 μ F ceramics. The filter capacitors with “B” priority, the reference filter to stabilize the reference voltage for internal Ops and reference output filters should be placed close to USB audio controller. A good reference voltage is relative to good analog performance. These decoupling capacitors should be close to the USB audio controller pins (Audio input pin), or positioned for the shortest connections to pins, with wide traces to reduce impedance.

3.5 The USB connector

Place the USB device and connector on the un-routed board first. With minimum trace lengths, as equal as possible (D+, D-), route full-speed clock and USB differential signal pair first. Keep the distance between full-speed signals to USB differential signal pair far. Route the USB differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change. If it's necessary to turn 90°, it's better to use two 45° turn or an arc instead of making a single 90° turn. It can reduce reflection

on the signal by minimizing impedance discontinuities.

Please don't route USB differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference. Stubs on USB differential signal pair should be avoided. While stubs exist, it will cause signal reflection and lower the quality. If a stub is unavoidable in the design, no stub should be bigger than 200mils.

3.6 Guard ring on PCB-edges

The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. As shown in Figure 10 the field lines of the signal return to PCB ground as long as an "infinite" ground is available. Traces near the PCB-edges do not have this "infinite" ground and therefore may radiate more than others. Thus signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or - if not avoidable - should be accompanied by a guard ring on the PCB edge.

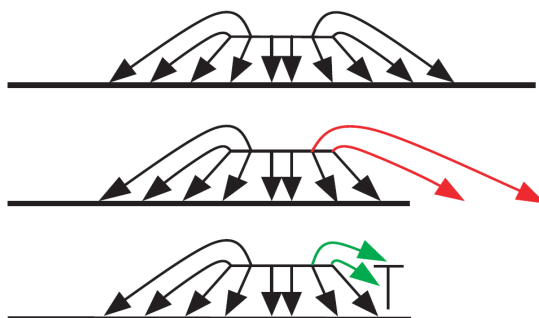


Figure16. The field lines of signal return to PCB ground.

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 10. As these traces should have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

Advantages of power planes

1. Easy and fast to implement
2. Low inductive power supply
3. Creates a capacity together with ground plane

Advantages of routed power supplies

1. Allows the usage of one layer for more than one supply system, thereby reducing the cross-talk between these supplies
2. May reduce cross-talk within each supply system
3. Requires more careful power routing
4. Higher supply impedance may require extra capacity for supply stabilization.

The optimum obviously is to apply the advantages of both methods. Therefore several local power planes should be implemented and connected to the supply via traces. Planes of different supply systems should be located in the same layer or separated by a ground plane to minimize crosstalk between these systems. Although the local power planes are easy to implement special care must be taken when connecting the power pins and the decoupling capacities to the planes.

(a) Connection of decoupling capacities

The decoupling of the most critical power supply pins of the microcontroller (for identification of these refer to chapter 3) very often is the most fastidious part in a PCB design. Even in a multilayer design every millimeter of trace has to be carefully considered.

(b) Sketch equivalent circuits

When considering the best placement, direction and connection of the capacity a small sketch may be very useful. Each piece of wire shall be drawn as impedance even though the actual value is not important. The Figure 11 clearly indicates that the 2 red impedances should be minimized while the other 2 may be object to concessions.

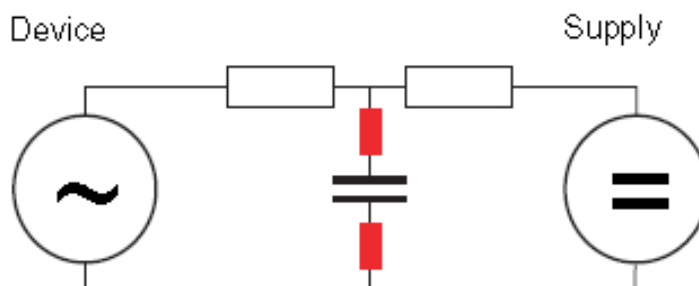


Figure17. Sketch equivalent circuit.

3.7 Cross Talk

A VIA has a considerable impedance

As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The 2 parts of next Figure indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.

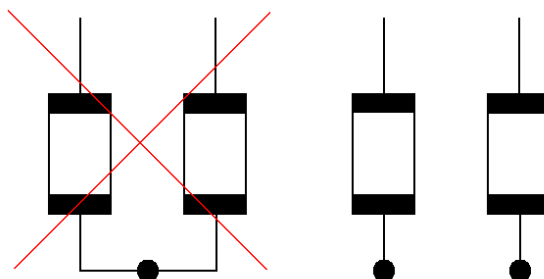


Figure18. Bad screw hole to Cross-Talk.

3.8 Return Current and Loop Areas

Image Planes

Return path or image planes provide low impedance, shortest possible path for return signal currents. The best image plane is the ground plane for the Cmedia USB Audio board.

Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

Avoid crossing the image power or ground plane boundaries with full-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane.

An electrical circuit must always be a closed loop. Up to now, only the signal path was discussed but not the path back to the source - the return current. With DC, the

return current takes the way back with the lowest resistance. With a higher frequency, the return current flows along the lowest impedance. This is directly beside the signal.

If this return path, mostly the ground plane, has a slot, the return current has to take another way and the results in a loop area. The larger the area, the more radiation and EMI problems occur. The designer has to make sure that the return current can flow directly underneath the signal trace. Another is to route the signal the same way as the return current flows.

3.9 ESD Protection System Design Consideration

ESD protection system design consideration is covered of the CM6531N's PCB.

- The following are additional considerations for ESD protection in a system.
- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy

4 Preset EQ Modes

As mentioned above, the EQ engine provides 4 preset EQ modes for different user scenarios/applications. Customers can use EEPROM parameters to change the gain of each band of the 4-preset EQ curves according to their needs. Users can use the hardware switch on the product (determined by 2 EQ configuration input pins) to change different EQ mode:

a. Default/Music mode (EQ_SEL0=0, EQ_SEL1=0)

- Flat frequency response
- Keep high-fidelity original audio
- Suitable for music listening or normal usage

b. Gaming mode (EQ_SEL0=0, EQ_SEL1=1)

- Enhance deep and rich bass effects in games
- Experience more realistic bombing, firing and ambient sounds
- Fit best for PC game-play

c. Communication mode (EQ_SEL0=1, EQ_SEL1=0)

- Suppress low and high frequency noises
- Enhance your voice clarity in communication
- Optimized typically for TIA920/UC telephony standard
- Fit only for PC VOIP applications

d. Movies mode (EQ_SEL0=1, EQ_SEL1=1)

- Enhance the common audio bands in movies or music
- Compensate the weakness of common headphone SPL/frequency characteristics
- Recommended for Movies mode if 4-modes are provided
- Recommended alternative for Default/Music mode (mode 1) for improving headphone driver's performance

Record path also support EQ function. It needs firmware support.

— End of Data —

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