HS-100C
USB Audio Single Chip

Application Notes

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Release Note

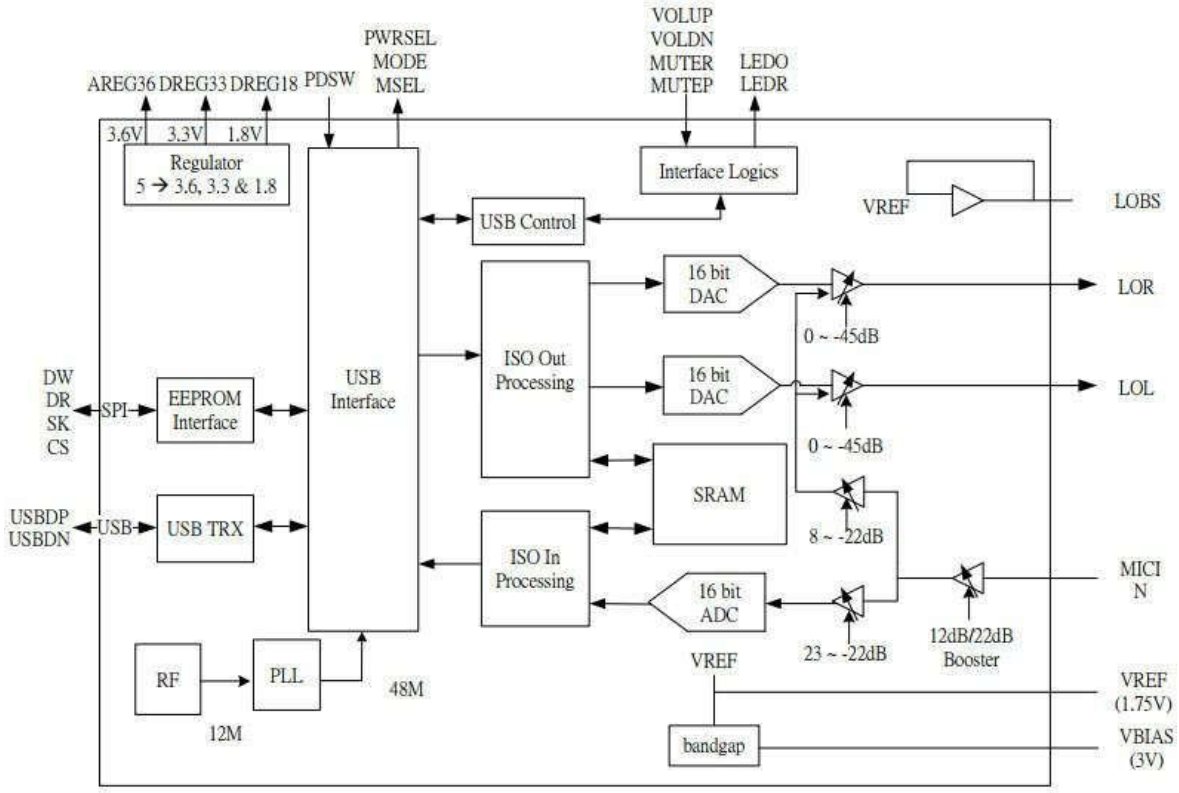
Revision	Date	Description
1.00	2021/07/26	Preliminary release
1.10	2022/05/03	Add 4.2 Differential Signal Pair Impedance Matching

1 About this document

This document summarizes the common application notes for customers who are designing their products with Cmedia HS-100C USB audio single chip solutions. It contains the system block diagram, schematics design notes, layout guide, and some other design notes. It's recommended to read this document before starting to plan and design products with HS-100C USB audio solution.

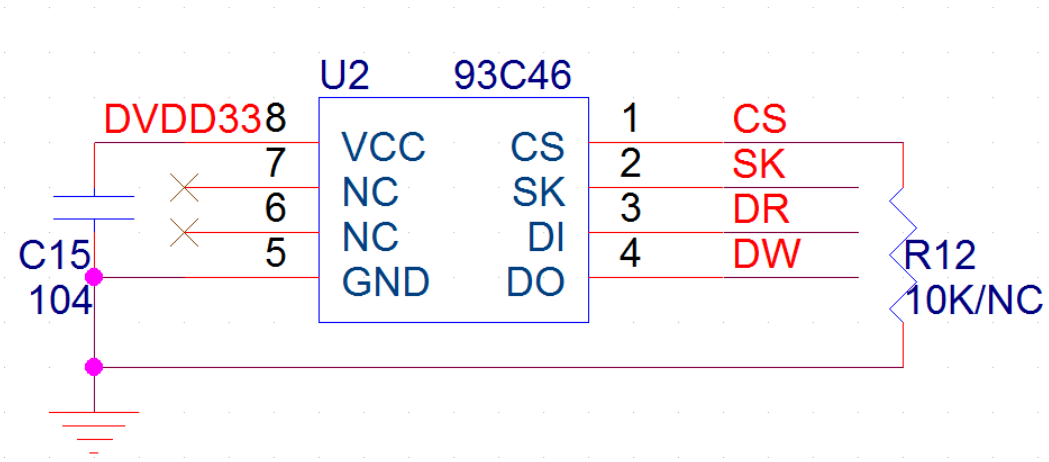
2 Typical IC Block Diagram

The typical IC block diagram is as following:



3 Schematics Design Notes

3.1 EEPROM



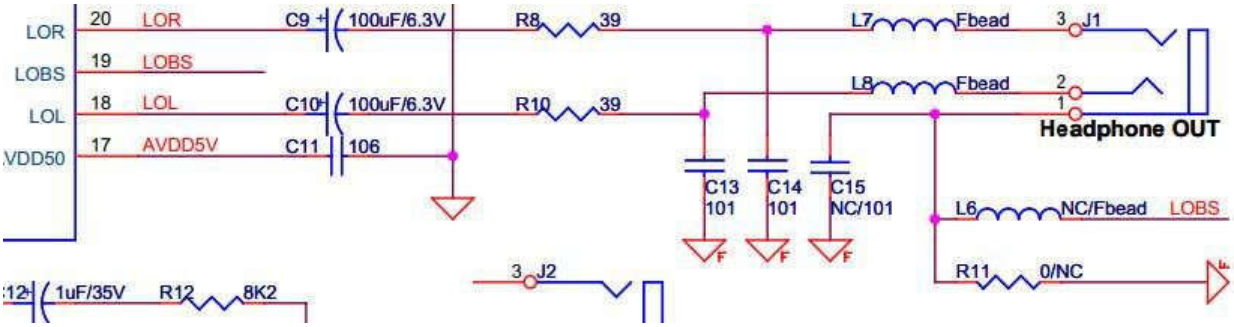
HS-100C support EEPROM 93C46.

Multiple settings are available by changing the parameters of the EEPROM.

For more information, please refer to the EEPROM configuration tool and its user manual.

The 10K ohm resistor shown in the figure might need to be placed. It depends on the reference circuit in the datasheets of different EEPROM manufacturers.

3.2 Headphone Out for Cap-less Design

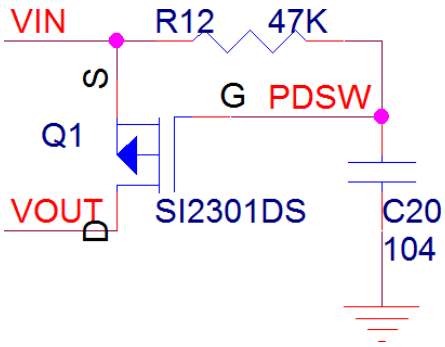


HS-100C support Cap-less Outputs.

For lower capacitor component cost, C9 and C10 can be removed (short-circuited), and use cap-less line out as the schematics above. However, when using cap-less mode, the inter-channel crosstalk may be slightly higher (worse).

Output Type	R11	C15	C9	C10	L6
Normal	Short	Open	100uF	100uF	Open
Cap-less	Open	101	Short	Short	FBead

3.3 Power Control Design

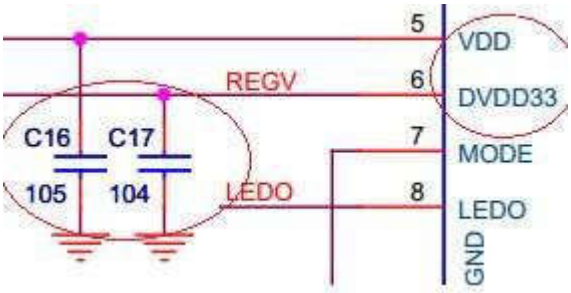


PDSW power control supports DC 1.8V ~ 5V

OS Mode	PDSW state
Operation	Drive Low
Suspend	Open

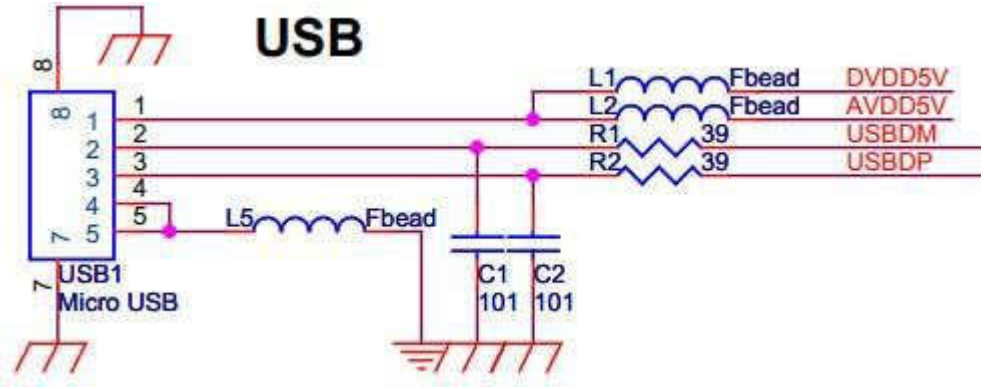
Please place a capacitor as C20 for a more steady system if the external circuit requires a current more than 100 mA.

3.4 Crystal-less Design



HS-100C embedded an internal cost effective oscillator. Therefore, no other external crystal or oscillator is needed. For better performance and steady system, please place a 1uF (105) capacitor for VDD and 0.1uF (104) for DVDD33 regulator pins.

3.5 USB Interface Design



R1 & R2 are for USB PHY impedance matching.

C1 & C2, L1,L2 & L5 are for EMI solution.

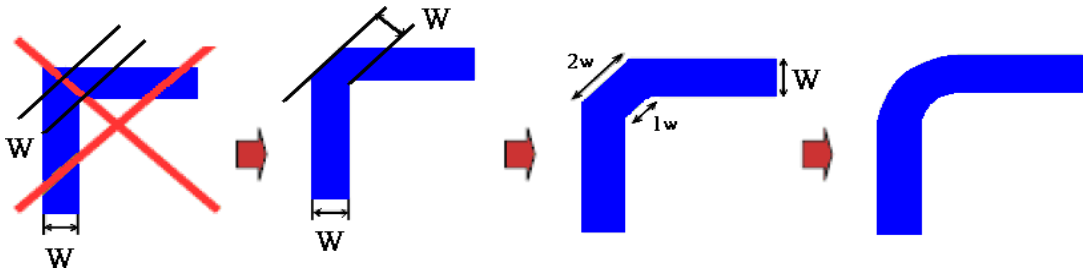
No pull up resistor is needed for USBDP since it's embedded in the internal PHY circuit

4 Layout Guide

This section provides guideline for the design of high integrated USB audio PCB. It's important to ensure maximum performance proper component placement and routing. This document includes properly isolated digital circuit and analog circuit. The effects of ground loop and supply plane geometry, decoupling/ bypassing/ filtering capacitors placement priorities, USB D+ and D- signals, analog power supplies, and analog ground planes.

4.1 General Rules

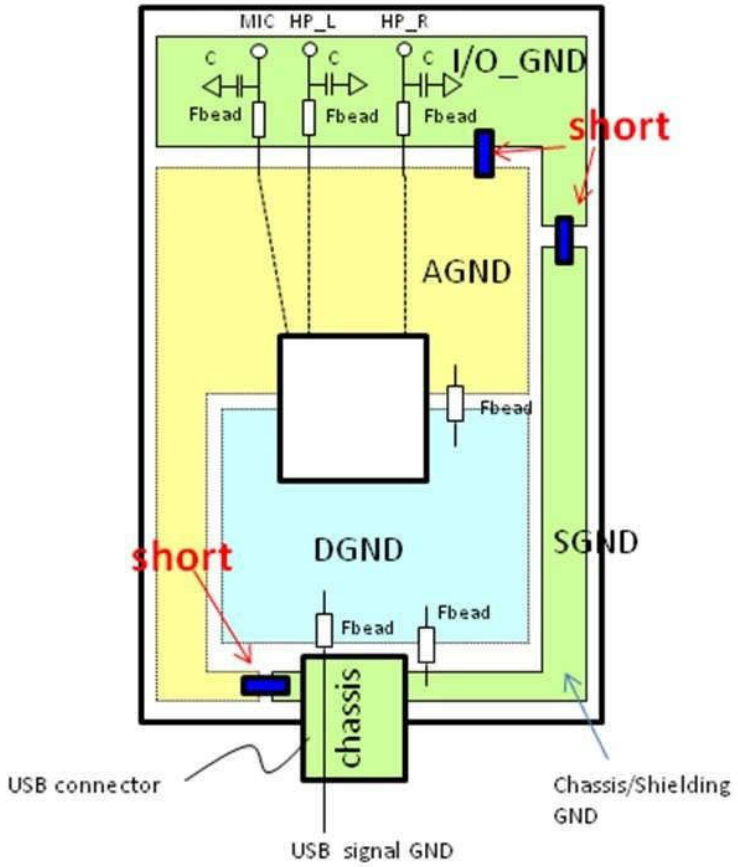
1. If a path has to turn 90°, it's better to separate the 90°into 2 turns by using two 135° turn (keep angles >= 135°) or an arc instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.

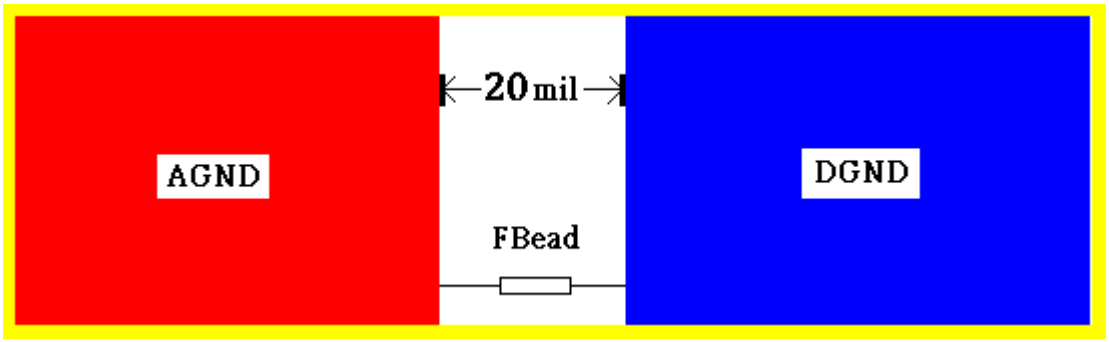


Turn Angle

2. The old rules of splitting power and ground into “digital” and “analog” sections is necessary when doing an audio PCB layout. If possible, analog circuit and analog power should be put on Analog ground area, and digital ones are separate from the analog area.

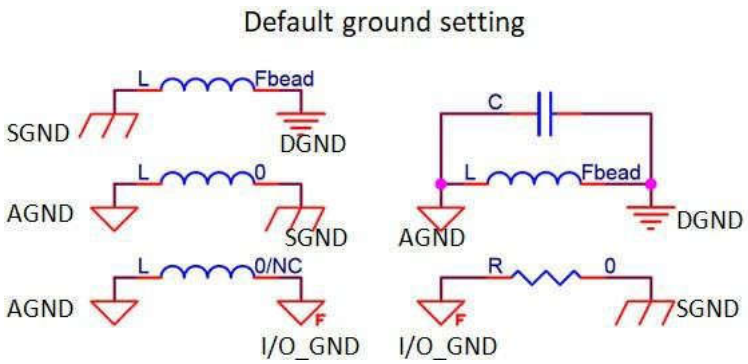
3. It is recommended to use 4 grounds when building a grounding system: AGND / DGND / USB Shielding ground (SGND) / IO ground (I/O_GND). Use different ferrite beads or resistors to connect different ground planes when debugging EMI issues.





AGND and DGND

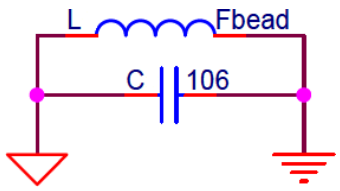
AGND: Analog GND
DGND: Digital GND
SGND: System/Shielding GND
I/O_GND: Phone Jack GND.



A. Short between AGND and I/O_GND, EMI could degrade, but crosstalk (between headphone out to microphone in) could improve
   Adding a bead between AGND and IO_GND, EMI could improve, but crosstalk (between headphone out to microphone in) could degrade
B. Short between SGND and I/O_GND, could improve ESD, but ground noise could induce from USB shielding
   Adding a bead between SGND and I/O_GND, could degrade ESD, but become less susceptible to USB shielding noise
C. In some case, AGND and IO_GND could be merged as AGND*. Short between AGND* and SGND could improve ESD, but could induce USB shielding noise, if shielding is not properly implemented
   Adding a bead between AGND* and SGND could degrade ESD, but become less susceptible to USB shielding noise

D. By default DGND and AGND is connected by a bead, and provides better audio quality. However if the PCB size is small, or ground area is already small, DGND and AGND could be short together to increase ground plane and improve ESD. The side effect is reduced in audio quality.

E. As shown in the diagram below, the capacitor (e.g. 10uF) connected between DGND and AGND is to reduce EMI



In general if PCB size is very small (for example, implemented to fit into USB type-C connector), it is recommended to connect all the grounds together to be effective. If the PCB size is large enough, it is recommended to separate different ground planes and short only the necessary parts according to issues to overcome (e.g. ESD, EMI and crosstalk)

4. Connect analog and digital power planes at one point through a low impedance bridge or preferably through a ferrite bead.

5. To achieve proper ESD/EMI performance; it's suggested to use a 0.1uF capacitor on each cable PWR bus line to chassis GND close to the connector pin. If voltage regulators are used, place a 0.1μF capacitor on both input and output. This is to increase the immunity to ESD and reduce EMI.

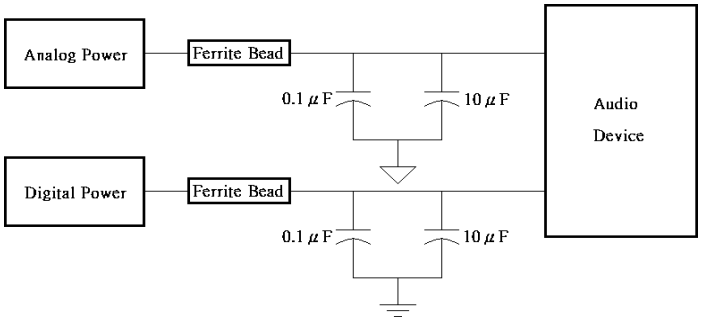


Figure6. Capacitors Array

6. Do not route traces cross from one power/ ground plane to another. This can cause a broke n RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

4.2 Differential Signal Pair Impedance Matching

The USB D+ D- differential pairs, which can operate at a rate of 12Mbit/s, are some of the most critical signals on a PCB. Its implementation on the PCB requires special considerations. The inductive and capacitive reactance, resistance, and conductance of a PCB differential pair will determine the impedance of the trace pair at any point along the PCB track. The value of differential impedance will be a function of the physical dimensions of the trace, as detail below.

Differential: Impedance of 90Ω, is optimal

Single-end: Impedance of 45Ω, is optimal

4.3 Layout design of Ground and Supply Plane geometry

The layout separates the analog and digital ground planes with a 20 to 30 mils gap. The moat helps to isolate noisy digital circuit from clean analog audio circuit. The digital and analog ground planes are tied together by a wide link(about 30mils) at a point close to the USB connector. This will be the "drawbridge" that goes across the moat. Do not allow any digital or analog signal traces pass through the drawbridge. Otherwise, the digital noise may get into the analog signals and make audio performance worse.

In order to achieve the best audio performance and prevent crosstalk issue, C-Media recommend that the width of each I/O signal trace be at least 10 mils and the space be at least one time the size of the width of signal trace.

For a layout that helps to reduce noise, separating analog and digital ground planes is needed. The digital components should be placed over the digital ground plane, and the analog components (including the analog power regulators) should be placed over the analog ground plane. In addition to ground planes scheme, digital and analog power

supply planes should be partitioned directly over their ground planes. Place analog power coincident with analog ground and digital power coincident with digital ground. If any portion of analog and digital plane overlaps, the distributed capacitance between the overlapping portions will couple digital noise into the analog circuit. This defeats the purpose of isolating the power planes. The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

4.4 Decoupling and bypassing capacitors

Bypass capacitors on the PCB are used to short digital noise to ground. Commonly, USB audio controller may generate noise when its internal digital circuit is operating. The current changes arise in the power and ground pins for the related section of the USB audio controller. The goal is to force AC current to flow in the shortest loop from the supply pin through the bypass cap and back into the USB audio controller through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the USB audio controller and the bypass capacitors when in the operating frequency of the USB audio controller. The long-trace will greater the inductance. To avoid long-trace inductance effects, use the shortest traces for bypass capacitors, with wide traces to reduce impedance. For the best performance, use supply bypass leads of less than one-half inch.

The USB audio controller power supply pins are need the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10μF surface mount devices are good if they are used in conjunction with 0.1μF ceramics. The filter capacitors with “B” priority, the reference filter to stabilize the reference voltage for internal Ops and reference output filters should be placed close to USB audio controller. A good reference voltage is relative to good analog performance. These decoupling capacitors should be close to the USB audio controller pins (Audio input pin), or positioned for the shortest connections to pins, with wide traces to reduce impedance.

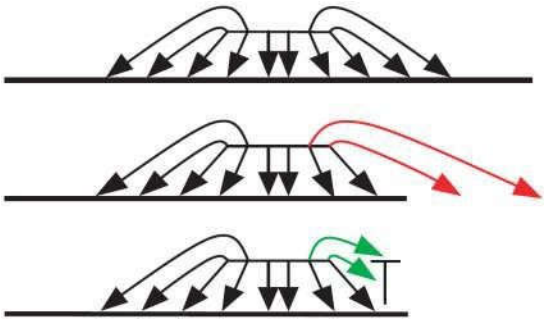
4.5 The USB connector

Place the USB device and connector on the un-routed board first. With minimum trace lengths, as equal as possible (D+, D-), route high-speed clock and USB differential signal pair first. Keep the distance between high-speed signals to USB differential signal pair far. Route the USB differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change. If it's necessary to turn 90°, it's better to use two 45° turn or an arc instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.

Please don't route USB differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference. Stubs on USB differential signal pair should be avoided. While stubs exist, it will cause signal reflection and lower the quality. If a stub is unavoidable in the design, no stub should be bigger than 200mils.

4.6 Guard ring on PCB-edges

The major advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. As shown in Figure 10 the field lines of the signal return to PCB ground as long as an "infinite" ground is available. Traces near the PCB-edges do not have this "infinite" ground and therefore may radiate more than others. Thus signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or - if not avoidable – should be accompanied by a guard ring on the PCB edge.



Fingure12. The field lines of the signal return to PCB ground

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 10. As these traces should have the same (HF) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

Advantages of power planes

1. Easy and fast to implement
2. Low inductive power supply
3. Creates a capacity together with ground plane

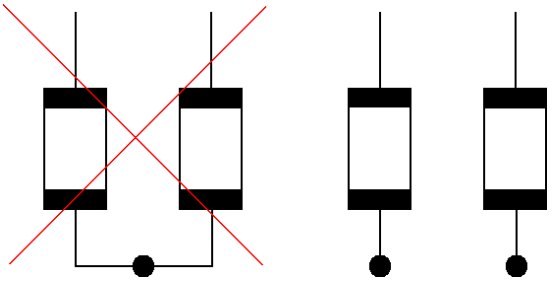
Advantages of routed power supplies

1. Allows the usage of one layer for more than one supply system, thereby reducing the crosstalk between these supplies
2. May reduce cross-talk within each supply system
3. Requires more careful power routing
4. Higher supply impedance may require extra capacity for supply stabilization.

4.7 Crosstalk

A VIA has a considerable impedance

As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The 2 parts of next Figure indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.



Fingure13. Bad Screw hole to Cross Talk

4.8 Return Current and Loop Areas

Return path or image planes provide low impedance, shortest possible path for return signal currents. The best image plane is the ground plane for the C-Media PCI Express board.

Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all

clock signals on the signal plane above a solid ground plane.

Avoid crossing the image power or ground plane boundaries with high-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane.

An electrical circuit must always be a closed loop. Up to now, only the signal path was discussed but not the path back to the source – the return current. With DC, the return current takes the way back with the lowest resistance. With a higher frequency, the return current flows along the lowest impedance. This is directly beside the signal.

If this return path, mostly the ground plane, has a slot, the return current has to take another way and the results in a loop area. The larger the area, the more radiation and EMI problems occur. The designer has to make sure that the return current can flow directly underneath the signal trace. Another is to route the signal the same way as the return current flows. The best solution is to avoid any slots in the d reference plane.

4.9 ESD Protection System Design Consideration

ESD protection system design consideration is covered HS-100C itself.

The following are additional considerations for ESD protection in a system.

· Metallic shielding for both ESD and EMI

· Chassis GND isolation from the board GND

· Air gap designed on board to absorb ESD energy

· Clamping diodes to absorb ESD energy

· Capacitors to divert ESD energy

4.10 EMI Solutions Summery

EMI issues can be very knotty and not easy to solve. However, with some tips and experience, it would be relatively easy when the debugger has some clues. Some tips are listed below for those who are dealing with EMI issues when making a USB audio device PCB layout.

·Build a 4-grounds ground system: AGND/DGND/IO_GND/USB Shielding GND and reserve a pad for resistor or fbead.

·Place at least a resistor/fbead pad for each analog output, since the EMI noise may be easily delivered through DAC paths.

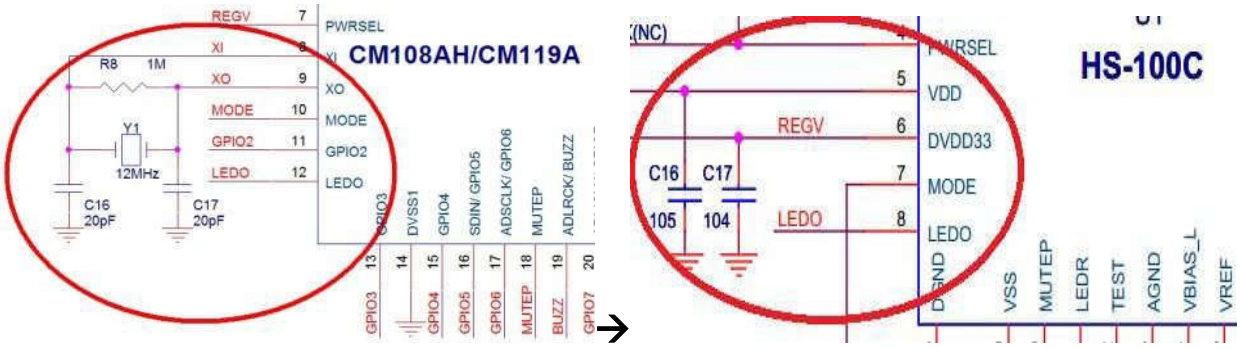
· If the frequency of measured over-limit-EMI-signal is 12MHz or its multiple (e.g. 36MHz/108MHz/132 MHz), it's more likely caused by the USB signal. Therefore, instead of modifying audio output/input paths, USB PHY related circuit needs to be considered.

5 HS-100C Transfer Guide

For those who are currently manufacturing products with HS-100C, this section highlights the parts that need to be noticed of the schematics.

5.1 Crystal/ No Crystal

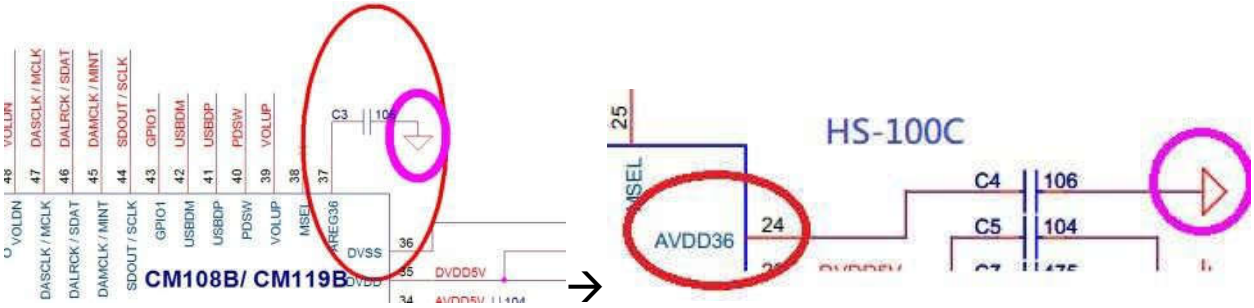
HS-100C uses internal cost effective oscillator, so PCBs designed for CM108AH/ CM119A/ HS-100 transferring to new HS-100C doesn't need an external 12MHz crystal oscillator. The original pins are replaced by digital regulator pins (3.3V & 1.8V) for external capacitors for steadier system. The differences and schematic modification of this part is shown in the following figures below.



5.2 AREG36/AVDD36

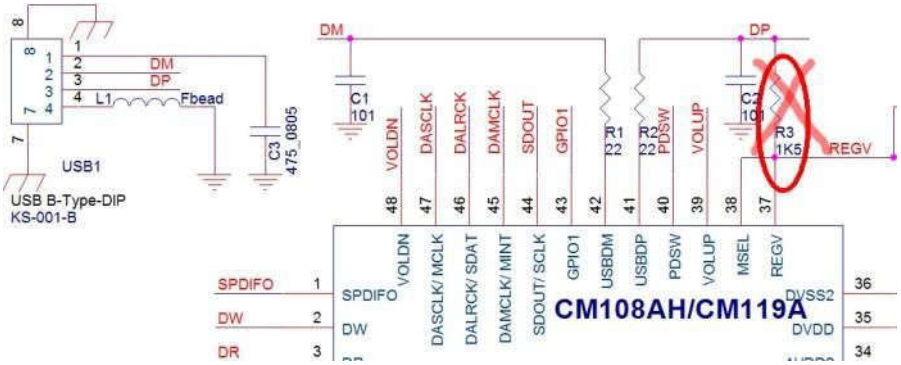
HS-100B/HS-100C replaced it with analog 3.6V regulator for better audio quality and performance.

The difference of this part is shown in the figures below.



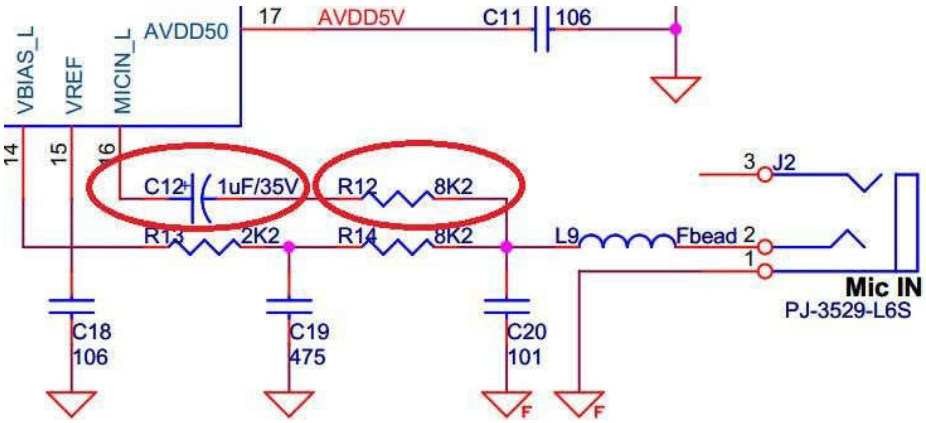
5.3 USB D+ Pull-up Resistor

When using HS-100C, the pull up resistor for USB D+ is not needed. The pull-up circuit is embedded in the USB PHY already.



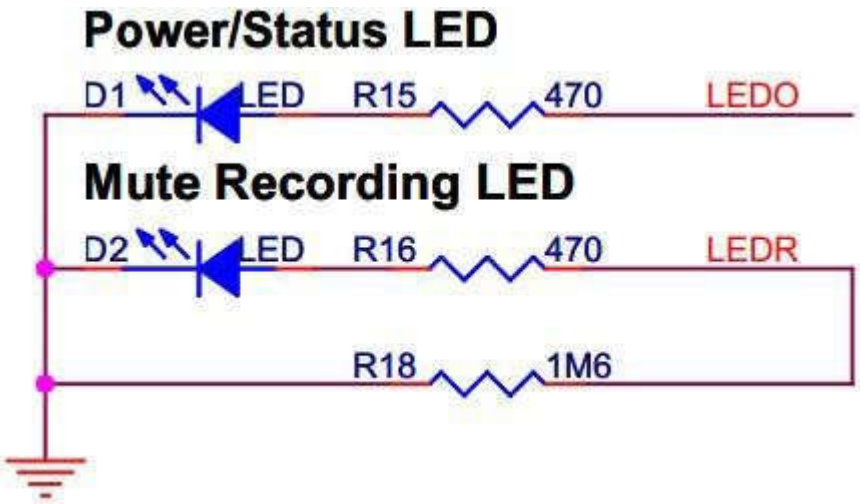
5.4 Microphone Input Design

HS-100C improved its ADC (MIC) performance, and it also has better sensitivity for microphones. For better voice recording quality, an 8.2K ohm resistor and a 1uF capacitor are placed (series connection) in the MIC path. The value of the resistor and capacitor may be slightly different for different PCB layout and microphones. Please follow the reference schematic for microphone section design.



5.5

Add R18 for recording mute LED flashing when IC power on.



Summary

The differences of CM108B/ CM119B/ HS-100B and HS-100C are summarized in the table below. Please check this table when designing products with HS-100C.

HS-100B:

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	DR	13	N.C.	25	AVSS	37	N.C.
2	DW	14	N.C.	26	VBIAS	38	N.C.
3	SK	15	N.C.	27	VREF	39	AVDD36
4	CS	16	N.C.	28	MICIN	40	MSEL
5	MUTER	17	MUTEP	29	AVDD	41	VOLUP
6	PWRSEL	18	N.C.	30	LOL	42	PDSW
7	VDD	19	LEDR	31	LOBS	43	USBDP
8	DVDD33	20	TEST	32	LOR	44	USBDM
9	N.C.	21	N.C.	33	AVSS	45	N.C.
10	MODE	22	N.C.	34	AVDD	46	N.C.
11	LEDO	23	N.C.	35	DVDD	47	VOLDN
12	DVSS	24	N.C.	36	DVSS	48	N.C.

HS-100C:

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	SK	13	AGND	25	MSEL
2	CS	14	VBIAS_L	26	VOLUP
3	MUTER	15	VREF_PAD	27	PDSW
4	PWRSEL	16	MICIN_L	28	USBDP
5	VDD	17	AVDD50	29	USBDM
6	DVDD33	18	LOL	30	VOLDN
7	MODE	19	LOBS	31	MISO
8	LEDO	20	LOR	32	MOSI
9	VSS	21	AGND		
10	MUTEP	22	AVDD50		
11	LEDR	23	DVDD50		
12	TEST	24	AVDD36		

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