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CM66XX

USB Hi-Speed Audio Layout Guide and Application Notes

Version: 1.0

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Revision	Date	notice
0.9	2018/12/03	First version
1.0	2018/12/18	Updated figures and description

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(一) About This Document

The purpose of this document is to summarize the common application notes for customers who are designing their products with Cmedia CM66XX USB2.0 audio controller series or who are evaluating the solutions. It will contain the following contents about the typical system block diagram, schematics design notes, layout guide, applicable PC OS, and exception notes. It's recommended to read this document before you start to plan and design your products with CM66XX USB2.0 audio solutions.

(二) CM66XX USB2.0 Audio Solutions Introduction

CM66XX are versatile true USB2.0 High-Speed audio controllers that are compatible with USB Audio Device Class v.2.0 specification. CM66XX support up to 768KHz and 16-32 bit audio data processing capability. They are embedded 8051 compatible MCU to become a programmable controllers for custom design and are very flexible for implementing various applications such as USB True HD headset, Microsoft OC devices, USB DAC, Headphone Amp or Speaker Amp, laptop docking stations, Hi-Fi Microphone or recording consoles, wireless audio, etc.. CM6212 supports Intel® HDA link and CM6637 support both I2S and HDA interfaces. Cmedia offers a total solution kit for CM6212 USB2.0 audio controllers with high-quality CM891 HDA codecs and also provide a reference design/firmware for CM6637/CM6635 with I2S DAC/ADC. To reach the high-quality and high bit-rate audio performance CM6637/CM6635 solutions even support feedback endpoints for output to get better data rate synchronization with PC USB host and lower clock jitter. The table below summarizes the turnkey solution offerings.

☰) CM66XX USB Hi-Speed Audio Layout Guide

CM66XX audio solutions are running on USB2.0 High-Speed bus and hence the PCB layout is very critical to the rapid digital signal transaction on the bus traces. This following section provides some guideline for the design of USB 2.0 high-speed audio print circuit boards, including general rules of implementation, impedance matching, component placement, trace routing and spacing considerations

(1) General Rule

1. If it's necessary to turn 90° angle of the trace, it's better to make two 45° turns or an arc, instead of making a single right-angle turn. It can reduce signal reflection by minimizing impedance discontinuities.

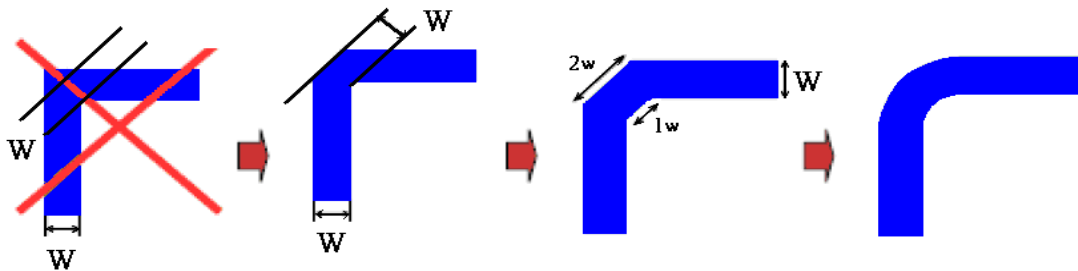


Fig.1 Turn Angle

- Put Analog GND and Analog POWER plane in the same region; place Digital GND and Digital POWER plane on other region.
- Use Ferrite Bead to connect different ground plane to avoid the EMI issue.
- Connect analog and digital power planes at one point through a low-impedance bridge or preferably through a ferrite bead as figure 2.

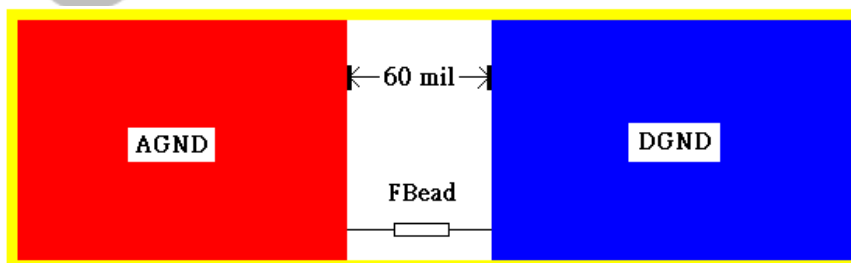


Fig.2 AGND and DGND

- Place some filter capacitors on power supply traces near OP-Amplifiers for cleaner power and audio

Signal-to-Noise Ratio.

6. If using capacitance 470uF、272uF、273uF in OP-Amplifier circuitry, select mylar or other material alike capacitors for better audio quality.
7. To achieve proper ESD/EMI performance, it's suggested to use a 0.1uF capacitor on each cable PWR bus line to chassis GND close to the USB connector pin. If voltage regulators are used, place a 0.1uF capacitor on both input and output. This is to increase the immunity to ESD and reduce EMI.

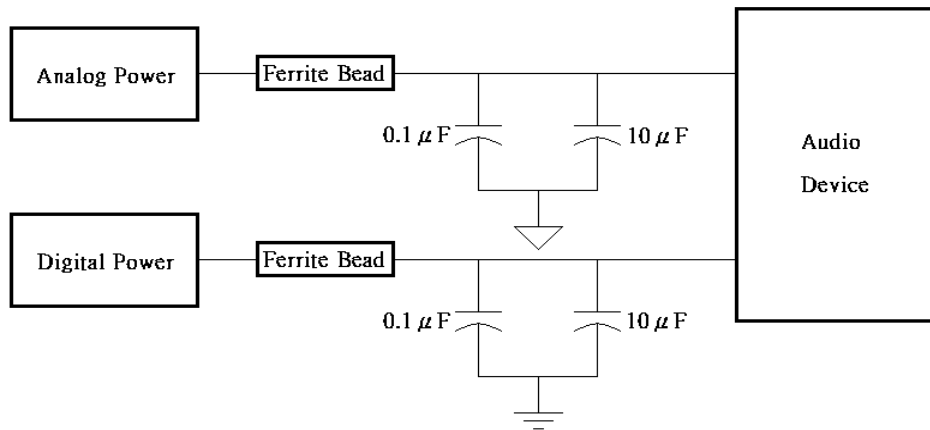


Fig.3 Capacitors Array

8. Do not route traces crossing one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it's best to run all clock signals on the signal plane above a solid ground plane

(2) Differential Signal Pair Impedance Matching

The USB 2.0 D+/D-differential signal pair, which can operate at a rate of 480Mbps (High-Speed), are some of the most critical signals on the PCB. Its implementation on the PCB requires special considerations. The inductive and capacitive reactance, resistance, and conductance of a PCB differential pair will determine the impedance of the trace pair at any point along the PCB track. The value of differential impedance will be a function of the physical dimensions of the trace, as details below. For a USB 2.0 differential pair, an impedance of 90Ω is optima.

(3) Placement and Routing Rules of Differential Signal Pair

1. Place the USB connector and the CM66XX audio chip on the unrouted board first. Route high-speed differential signal pair first with minimum trace lengths and as equal as possible (D+, D-). Keep appropriate distance between the USB 2.0 differential signal pair.
2. Route the USB 2.0 differential signal pair on the component side, which is adjacent to the ground plane layer. Vias to different signal trace layers or routing too close to breaks in the ground plane will adversely affect the differential trace impedance.
3. Route USB 2.0 differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change.
4. Please don't route USB 2.0 differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference.
5. Stubs on USB 2.0 differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality.
6. Route USB 2.0 differential signal pair traces over continuous ground and power planes. Avoid to cross anti-etching areas or any breaks in the underlying planes, or routing near the edge of the PCB or power planes.
7. Keep parallelism between D + and D-with the proper trace spacing to achieve 90Ω differential impedance.
8. Separate paths of SPDIF IN and OUT for at least 20 mils gap.
9. Do not allow any digital or analog signal traces pass through the drawbridge. Otherwise, the digital noise may induce into the analog signals, makes audio performance worse.
10. Avoid crossing the power or ground plane boundaries with high-speed clock signal trace up and down the separated planes. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through screw holes.

11. C-Media recommended to lay out the width of each signal traces at least 10 mils and the space is at least one time the size of width of signal trace.

12. For ADC and DAC, VREF connected capacitor is also for bypass. Depending upon the converter architecture, the range of the large capacitor may be from 1uF to 47uF. Place bypass capacitor as close to the chip as possible. Placement of the capacitors near the chips is very important. The bypass capacitors provide high speed current for the modulator operation, so the bypass capacitors are actually used to store charge for this high speed current draw.

(4) USB 2.0 Differential Signal Trace Spacing

The physical construction of differential PCB traces determines the differential impedance.

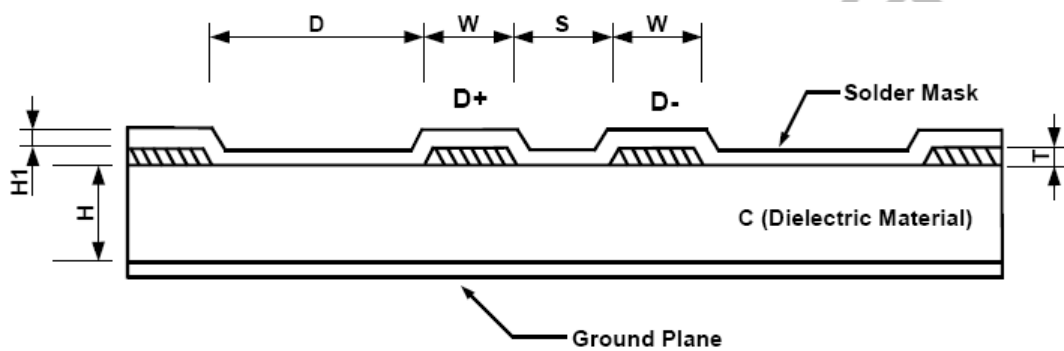


Fig.4 USB2.0 Differential Signal Trace Spacing

The primary physical characteristics are summarized as follows.

1. W = Width of the trace
2. S = Separation from D+ to D-
3. H = Dielectric thickness, distance from trace to the ground plane.
4. T = Thickness of the trace
5. D = Ground Separation
6. H1 = Solder mask thickness
7. Er = Dielectric constant (depend on C, example: FR4 Er =4.6)

The PCB designer should use an impedance calculator to determine the differential trace impedance of USB 2.0 differential signal pair. Note that the calculations to determine the differential impedance are somewhat different from those used to calculate the impedance of a signal trace.

Customers could just refer to Cmedia's layout files and the PCB stack-up parameters are as follows.

W =20 mils

S =30 mils

D ≥ 30 mils

H ≈ 9 mils

T = 1.4 mil

Er ≈ 4.6 (FR4 material)

Board thickness ≈ 63 mils (1.6 mm)

(5) PCB Stack-Up and Layering

In USB 2.0 applications, a PCB with a minimum of 4 layers is required. Because it needs to control the impedance of the USB 2.0 differential signal pair and supply a clear power and ground. The 4 layers are typically configured as below described.

1. Component Side (Top)

It contains differential signal pair and other signal routing and primary surface-mounted components.

2. Ground Layer

Ground plane (include AGND and DGND) . Also, is reference layer for differential signal pair.

3. Power Layer Power plane (include AVCC and DVCC) .

4. Solder Side (Bottom)

Contains signal routing and secondary surface-mounted components.

Layer	Description	Signification Features
1	Component Side (Top)	Contains differential signal pair and other signal routing and main components.
2	Ground Layer	Ground plane (include AGND and DGND).
3	Power Layer	Power plane (include AVDD and DVDD).
4	Bottom Side	Contains signal routing and other components.

Because of the high frequencies associated with the USB, PCB with at least four layers is recommended; two signal layers separated by a ground and power layer.

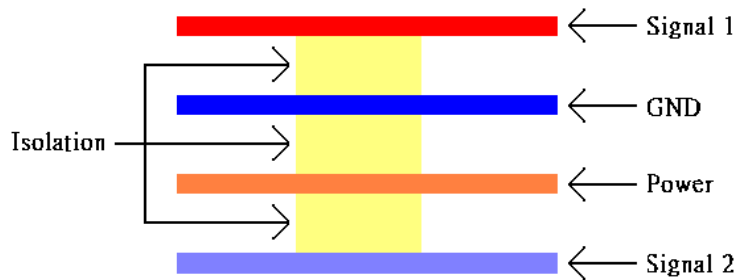


Fig.5 Four layer board

The majority of signal traces should run on a single layer, preferably signal1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

(四) CM66XX USB Hi-Speed Audio Application Notes

(1) Both crystal and oscillator selection

In crystal-based oscillator circuit, the oscillatory frequency is almost entirely based on the characteristics of the crystal. Therefore, it is important to select a crystal that meets the design requirements as below. The feedback resistor R has been used on the PCB. It is necessary to add feedback resistor (1M ohms) as figure 6.

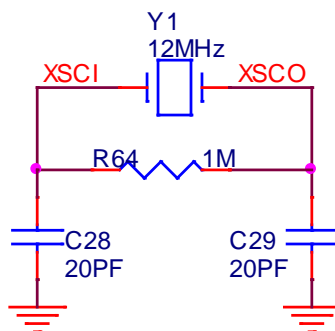


Fig.6 Crystal Circuit

Below is typical crystal specification of 12MHz, please note the tolerance of frequency and stability over temperature range and make sure start-up time around 2-5ms to ensure our system stability. Oscillator

selection, please also refer to below table.

Parameter	Typical Value
Nominal Frequency	12.000000MHz
Oscillation Mode	Fundamental
Frequency Tolerance	±30ppm
Load Capacitance	20pF
Shunt Capacitance	4~6pF(max7pF)
Effective Series Resistance	60ohms
Drive Level	100uW
Stability Over Temperature Range	30ppm
Operation Temperature Range	-10℃ ~ +70℃
Aging	±5ppm / year

The frequency tolerance shall be less than 30ppm. Load capacitance is a critical crystal parameter, which specifies the capacitive load that must be placed across the crystal pins to oscillate at the specified frequency. It influences the actual oscillation frequency, as the crystal manufacturer actually 'trims' the crystal to oscillate at its nominal frequency for the specified load capacitance. Note that the CL is the capacitance that the crystal needs to see from the oscillator circuit; and it is not the capacitance of the crystal itself.

From the crystal parameters, the following formula will calculate the required capacitance load for the crystal to oscillate on the desired frequency.

Note that the CL is the capacitance that the crystal needs to see from the oscillator circuit; and it is not the capacitance of the crystal itself. From the crystal parameters, the following formula will calculate the required capacitance load for the crystal to oscillate on the desired frequency.

$$CL = C1 \times C2 / (C1 + C2) + Cs (+Ci)$$

CL: Load Capacitance ~20pF

Cs: Crystal Shunt Capacitance between XTAL In/Out pins ~7pF

Ci: IC Package Capacitance (LQFP-48 chip package is usually ~4pF)

Based on the load capacitance formula and crystal specification, it is recommended to use a crystal (12MHz)

with parameter of $CL = 20\text{pF}$ and $Cs = < 7\text{pF}$. The RESR of crystal must be 100ohms or less. Then the calculated external C1/C2 capacitors should be $\sim 20\text{pF}$ (18pF to 22pF) excluding the consideration of onboard parasitic capacitance.

When oscillator is used as the source of clock, the scheme is recommended as figure 7.

In clock input source, CM66XX can only use a 12MHz crystal because the ICs have embedded a PLL circuit.

Currently the CM66XX can also support 49.152MHz/24.576MHz (for 48kHz) and 45.1584MHz 22.5792MHz (for 44.1kHz) oscillator which may enhance audio quality due to the clock jitter improving.

CM66XX require a reset signal after power on. This is usually executed by an external circuit. If there is no the external circuit to provide a reset signal to the CM66XX, that digital status is unknown at power on. Reset is initiated by taking the high for at least 1ms.

Figure 7 illustrates a simple power-on reset circuit. When power on C1 charged, the PMOS turn on and then XRST up to 3.3V, system is reset. Then gate of PMOS is high, PMOS turn off, XRST down to 0V, complete reset cycle. XRST will reach 2ms approximately.

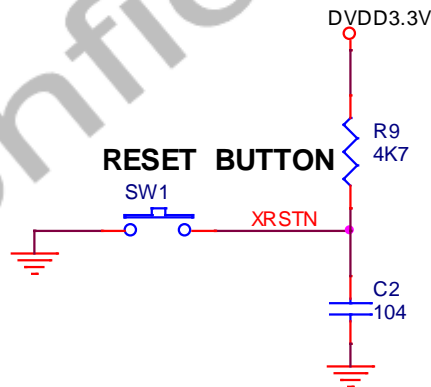


Fig.7 Reset Circuit

CM66XX series don't require a reset circuit because the series IC of CM66XX have embedded a power on reset circuit. The reset circuit as figure 8 can be removed, but CM66XX platform need keep this reset circuit.

(2) Negative Voltage

Most audio systems use switching power supplies to reduce costs. These power circuits introduce more noise than linear power. As the noise from switching power supplies increases, the trade-off between single-end and differential circuits start to blur.

Differential output DAC's are more expensive than single-end versions normally. In a typical DAC's amplifier circuits of CM66XX, the first stage is current to voltage converter, the second stage changes to a differential to single-end converter. For higher audio performance, application circuit use switching power and linear power.

Designers must consider several topics when designing a PCB layout for a dc-to-dc converter. The power stage in this application report is defined to include the input capacitors, power MOSFETs, driver IC, output capacitors and output inductor.

(3) Passive Component Selection

Selection of passive components can have a profound effect on both sound quality and specification realization. Care must be taken to match the types of passive components with the end product objective.

Bypass Capacitor

1. The basic definition of a bypass capacitor is that it is used to conduct AC components in the power supply line around the data converter circuit. This AC component is removed from the DC supply, enabling the converter to achieve its stated performance specification. Failure to adequately remove AC noise from the power supply line will allow the noise to couple into the converter, resulting in dynamic performance reduction.
2. Power supplies require that at least two capacitors for bypassing: a large capacitor (Nominally $>10\mu\text{F}$) for low frequencies noise and a small capacitor (nominally $=0.1\mu\text{F}$) for high frequencies noise. The actual value of the capacitors depends upon the noise characteristics of the power supply. If the noise is low frequency, increase the value of the large capacitor. If the noise is high frequency, add an additional capacitor with a smaller value than the previously selected small capacitor.

Capacitors

For power supply bypass capacitors and DC-blocking, we recommend using aluminum electrolytic. These capacitors open when they fail, they will prevent catastrophic system failures. However, at low temperature some low-grade electrolytic capacitors degrade in capacitance, resulting in high distortion.

Tantalum capacitors should be avoided for bypassing, they will short when they fail.

For filter capacitors that are in line with the audio signals, polypropylene film capacitors provide the best THD performance. The filter capacitor should use the ceramics, which can induce piezoelectric effects into the system.

Resistors

There are two types of resistors to consider: carbon and metal film. Each type has its advantages, depending on the primary objectives for the system performance. If sound quality is the top objective, we recommend using carbon film resistors. To maximize performance specifications (SNR and THD), you should use metal film resistors.

(4) Coupling Capacitor

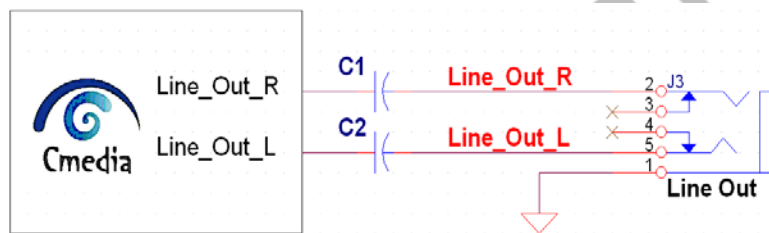


Fig.8 DC coupling Capacitor

Both C1 and C2 are coupling capacitors as figure 8. The purposes of capacitors are to isolate DC and pass AC. The coupling capacitors must have low inductance and low equivalent series resistance (ESR). All analog input/output path width must have up 20mils and separate AGND.

(6) OPA low pass filter

If use filter capacitors in OP-Amplifier circuit as figure 9, we have to select NPO capacitors or alike Mylar capacitors and resistors need select 1%-0.1% precision resistance to get good THD+N quality.

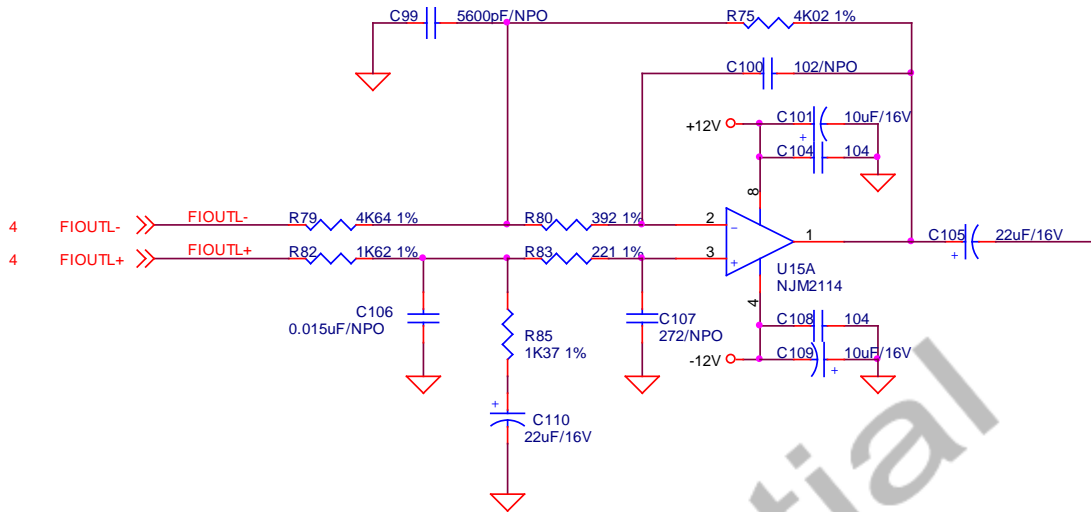


Fig.9 Low pass filter use NPO or Mylar capacitors and 1% resistor

(7) Cross Talk

The Figure 10 indication 2 components share a VIA which may cause 2 channel audio signal cross-talk, when your device has multi-channel audio signal, please avoid to share a VIA in the left and right circuit.

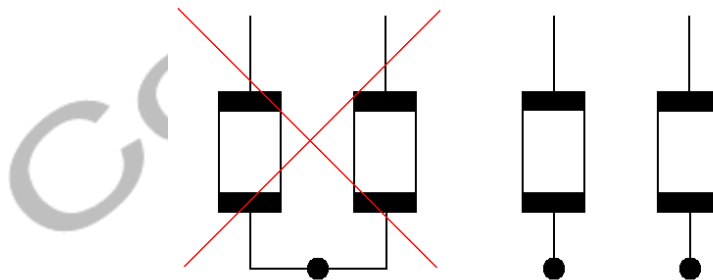


Fig.10 VIA cause cross-talk

(8) ESD Protection System Design Consideration

ESD protection system design consideration is covered of the CM66XX PCB. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND

- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy
- The use of external ESD components on the DP/DM lines may affect signal quality and is not recommended.

(9) Single Input to Differential Input

ADCs have differential (balanced) input. If your design needs to convert a single-end input to a differential input, please consider to use below figure 11 circuit or the application schematics of datasheet.

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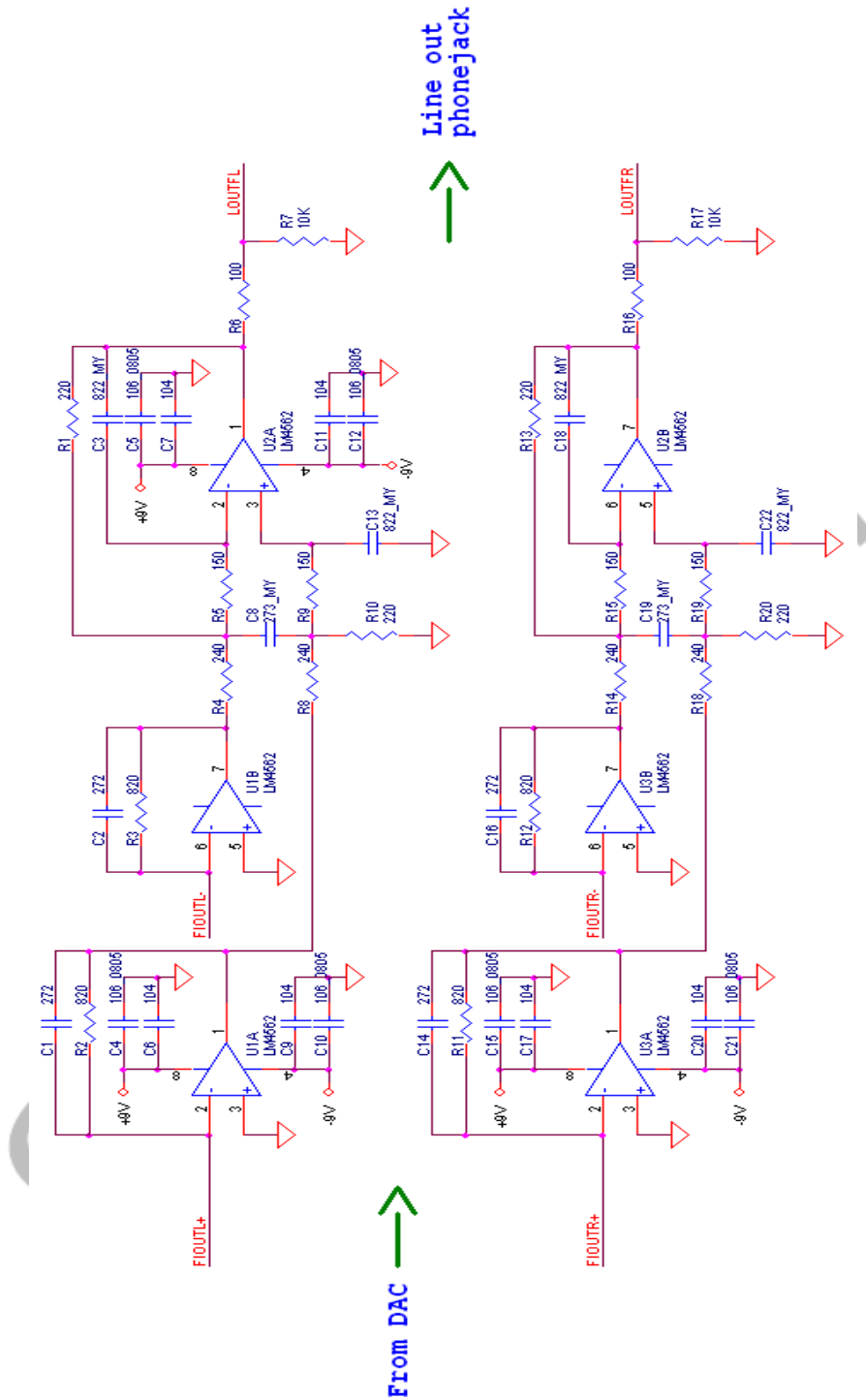


Fig.12 DAC Converter differential to single end

(10) Device with Self power or Bus power mode

According to our demo board design, CM6637/CM6635 is defined self power mode and CM6212 is defined bus power mode. If you want to focus in self power mode, please refer to below notes and reference circuit.

The figure 16 circuit is for self power only. If our device has different power source, then we need to choose a power mode which can be self power mode or bus power mode. If we use self power mode to test USB IF, then below circuit may consider design to our device for self power mode only.

(11) Anti-pop noise mute circuit

We recommended two kinds of solutions to mute pop noise in this application notes.

(1) The relay circuit can effectively avoid the pop noise and THD+N can also keep the original audio quality. Please reserve a GPIO (XGPIO_11) pin to control NMOS (Figure 19) which active is low. Now the CM66XX demo board of c-media has been enabled the relay mute circuit as figure 13, but hasn't enabled 8 channel pop noise mute function. If you don't care the pop noise, please remove the components of relay circuit and hand soldering R132 and R133 resistors.

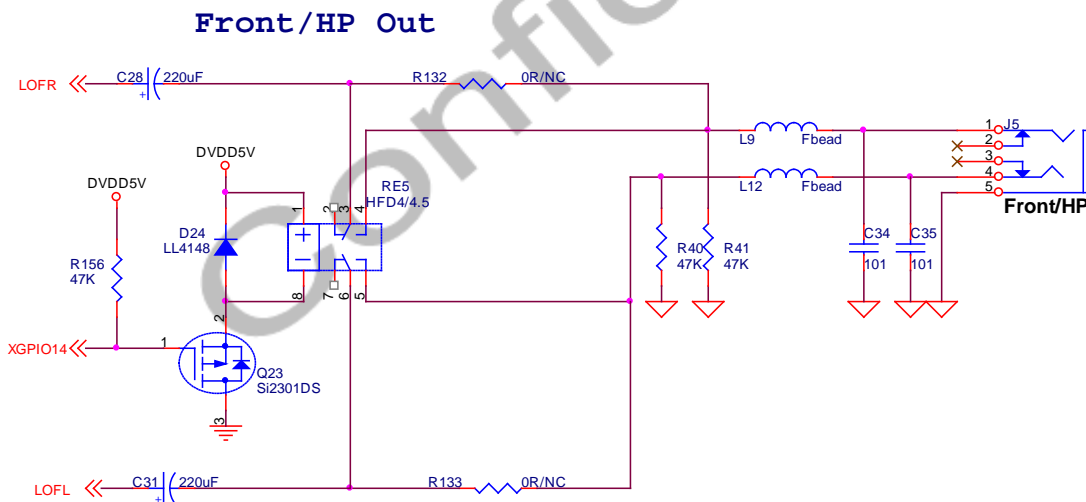


Fig.13 2 channel relay mute control circuit

(2) The advantage of MOS circuit is low cost design but it may affect the quality of THD+N. Every channel has dual NMOS transistors in series to avoid the pop noise. Now the CM66XX demo board of c-media hasn't mounted dual NMOS transistors and resistor components, so NMOS mute function is disabled.

Currently the mute control circuit needs a GPIO pin to control high or low of NMOS or transistor, thus you can

consider to use a pin GPIO to control all mute circuits or use two pins of GPIO to control 2 set mute control circuits as figure 13 and 14.

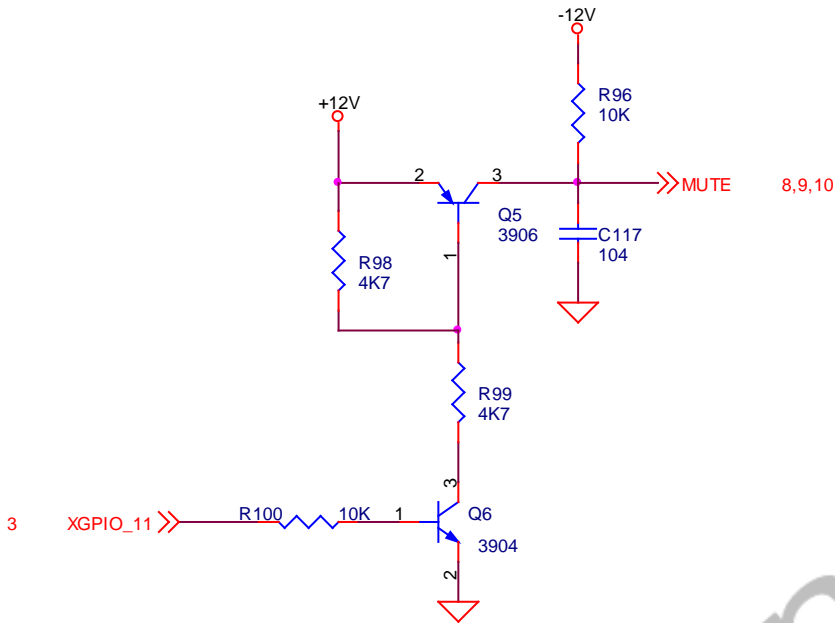


Fig.14 8 channel mute control circuit

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